WHAT IS CLAIMED IS:

1. A method of manufacturing an integrated circuit having trench isolation regions in a substrate, the method comprising:

forming a mask layer above the substrate;

selectively etching the mask layer to form apertures associated with locations of the trench isolation regions;

forming trenches in the substrate at the locations;

forming first type liners on first side walls of the trenches associated with first type regions of the substrate; and

forming second type liners on second side walls of the trenches associated with second type regions.

2. The method of claim 1, further comprising providing an insulative material in the trenches to form the trench isolation regions.

3. The method of claim 2, further comprising removing the insulative material until the silicon nitride layer is reached.

4. The method of claim 1, wherein the first type liners are a first thickness and the second type liners are a second thickness, the second thickness being different than the first thickness.

5. The method of claim 1, wherein the first type liners are dry oxide material and the second type liners are dry heavily nitrided oxide material.

6. The method of claim 1, wherein the substrate is on SOI substrate.

7. The method of claim 1, wherein the substrate trenches reach a buried insulative layer of the substrate.

8. The method of claim 1, wherein the substrate includes a strained layer, wherein the strained layer includes the first type region and the second type region.

9. A method of forming trench isolation liners in a CMOS IC, the method comprising:

forming a trench in a layer above a substrate or in the substrate, the trench separating a first doped region from a second doped region;

forming a first liner for a first side wall in the trench, the first side wall being associated with the first doped region; and

forming a second liner for a second side wall of the trench, the second side wall associated with the second doped region;

10. The method of claim 9, wherein the substrate includes a strained silicon layer, whereby stress in the first doped region and the second doped region is more equalized due to the first liner and the second liner.

11. The method of claim 10, wherein the first doped region is P-type doped with N-type dopants and the second doped region is doped with doped dopants.

12. The method of claim 9, wherein the first and second liners are oxide liners.

13. The method of claim 12, wherein the first liner includes oxygen.

14. The method of claim 13, wherein the second liner includes nitrogen.

15. The method of claim 14, wherein the substrate is a bulk substrate.

16. The method of claim 15, wherein the first liner provides relatively equivalent stress to the first doped region as the second liner provides to the second doped region.

17. An integrated circuit, comprising:

a first doped region of a substrate; a second doped region of the substrate;

a first liner on a first side wall of a trench, the trench being between the first doped region and the second doped region; and

a second liner on a second side wall of the trench.

18. The integrated circuit of claim 17, wherein the first liner is formed using nitrogen.

19. The method of claim 18, wherein the first and second liners are formed utilizing an oxygen atmosphere.

20. The method of claim 19, wherein the first liner is less than 400 Å thick.